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EXAMINER	
CEHIC, KENAN	

ART UNIT	PAPER NUMBER
2473	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,346	SPENCER, ANTHONY	
	Examiner	Art Unit	
	KENAN CEHIC	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 7-19, ,21-27, 29-39 and 42-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-19, ,21-27, 29-39 and 42-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. Claims 47 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. "A computer readable medium " can be a signal per se. It is suggested to change this to – A non-transitory computer readable medium--

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-19, 21-39, 42-55 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For claim 1, and similarly claims 22, 42-45, 47, 56, 60, recite a limitation where a **sole** / **single queue** handles / records **all packet records** that enter the system. The examiner fails to see support in the originally filled specification that there only a sole/single queue is used for storing / handling all packets records in a system. The specification appears to merely describe that queuing means processes packet records in the system. While the original filled claims disclosed that the queue means can be a

single queue, this queue means is used for storing packets and not all packet records entering the system as the claims currently recite. Further, the applicant fails to point out written support for newly amendment limitations in the response.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham **v.** John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2,5, 7, 8, 11, 22, 23, 26, 27, 29, 32, 42-45, 47, 56, 58-30, 62,63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) in view of Brunheroto et al (US 6,643,298) and Kiremdjian et al. (US 2003/0081623)

For claim 1 and similarly 22, 42, 43-45, 47 Sindhu discloses A sorting incoming data packets (see fig. 5; 70; col 7 line 55 through col 8 line 15 "receives data packets…divides the packets into cells…writes them to memory system"), the system comprising assignment means (see col 10 line 10-50 "request generator"), operable only on packet records containing information about said packets, for assigning an exit order to said packets (see col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet) ;

queue for handling all packet records which enter said system (see figure 7 , 88 / fig. 9; 104; col 10 lines 10-35 "header queues 104 responsive to said assignment means (see fig 5; 59; fig. 6, 85; fig. 8; 94; queue handle packet records of system) for storing and

arranging queuing said packet records sorted packets for output in said exit order (see col 10 line 10-50 “plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 “Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels”; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet);, and

memory means for storing said packets or data portions (see fig. 5; 76; col 7 line 55 through col 8 line 15 “receives data packets…divides the packets into cells…writes them to memory system 76”) thereof wherein said data portions being output from the memory means in accordance with the corresponding packet records being output from the queue means (see col 10 lines 10-50 “identifies an appropriate header queue 104 to obtain the address of the next data cell stored in memory...cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory”; cells of the data packet is outputted according to the order of the packet headers (i.e. packet whose header is on top of queue gets outputted first) in queue 104)

For claim 2 and similarly 23 , Sindhu discloses assignment means (see col 10 line 10-50 "request generator") is responsive to information contained within a packet whereby to determine an exit order number for that packet (see col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet)

For claim 5 and similarly 26, Sindhu discloses assignment means (see col 10 line 10-50 "request generator") is adapted to insert sorted packet records in said queue means in exit order (see col 6 lines 35-50 "data cell includes a header portion…: col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded

into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory")

For claim 11 and similarly 32, Sindhu discloses assignment means comprises a processor (see col 10 line 10-50 "request generator")

For claims 42, and 44 A computer system (see figs 1-7; col 19-20 "programmed..programming…software").

For claim 43, and 45 a network processing system (see figs. 1-6)

For claim 47, A computer readable medium containing instructions (see figs 1-7; col 19-20 "programmed..programming…software").

For claim 56 and similarly 60, Sindhu discloses a system for sorting and storing incoming data

packets comprising:

an input port (see figure 7; 85, 88); which receives record portions of said incoming data packets in an input order (see col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include

priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet);

an assignment processor (see col 10 line 10-50 "request generator") which operates on said record portions of said ncoming data packets to assign an exit order for said incoming data packets, wherein said exit order differs from said input order (see col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet; order that was in queue 88 can later be changed i.e. based on priority etc); and

a queue (see figure 7, 88, 9, 104), responsive to said assignment processor, for storing said record portions of all of said incoming data packets which enter said system (see figure 7 , 88 / fig. 9; 104; col 10 lines 10-35 "header queues 104 responsive to said assignment means (see fig 5; 59; fig. 6, 85; fig. 8; 94; queue handle packet records of system) in said exit order (see col 10 line 10-50 "plurality of header queues…sends the

packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet; order that was in queue 88 can later be changed i.e. based on priority etc).

For claim 58 and similarly 62, Sindhu discloses, further comprising:
an input device (see figure 6; 85), upstream of said input port, (see figure 6; 85) for receiving said incoming data packets (see figure 6; receives packets) and forwarding said record portions of said data packets to said input port (see figure 7; 88; queue receives headers from receive logic); and
a memory hub, connected to said input device (see figure 5; 76; col 8 lines 2-15; memory hub for packet data), for receiving and storing one of: (b) data portions of said incoming data packets (see figure 5; 76; col 8 lines 2-15; memory hub for packet data).

For claim 59 and similarly 63, Sindhu discloses an output device (see figure 9; 84), connected to said queue and said memory hub (see figure 9; 102, 104; fig. 5; 76) , for

outputting said data packets from said system in said exit order (see figure 9; 102, 104; fig. 5; 76; transmit logic outputs packets in the order as in queue 104).

Sindhu does not explicit discuss the following:

For claim 1 and similarly 22, 42, 43-45, 47, a sole queue for handling data; processing in real time

For claim 5 and 8, 26, 27 sole queue.

For claim 7 and 29, wherein said sole queue provides a plurality of virtual queues.

For claim 56 and similary 59, 60, 63, single queue

Brunheroto from the same or similar field of endeavor discloses the following features:

For claim 1 and similarly 22, 42, 43-45, 47, Brunheroto discloses processing in real time (see col 7 line 15-40 "real-time engine...packet header..."; col 6 lines 1-15 “real-time access" ; col 2 line 54 through 3 line 20 “real- time processing...real-time support”)

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu by using the above recited features, as taught by Brunheroto, in order to provide real-time processing of packets / headers in order to expedite and minimize delay when processing packets / headers in order to accommodate time critical data (see Brunheroto see col 2)

Kiremdjian from the same or similar field of endeavor discloses the following features:
For claim 1 and similarly 22, 42, 43-45, 47, Kiremdjian discloses a sole queue for handling data (see fig. 2a; section 0023 "single queue"; section 0035-42 "virtual…several entries.; see title; a single queue)

For claim 7 and 29, Kiremdjian discloses wherein said single queue provides a plurality of virtual queues (see fig. 2a; section 0023 "single queue"; section 0035-42 "virtual…several entries.; see title).
For claim 56 and similary 59, 60, 63, Kiremdjian discloses single queue (see fig. 2a; section 0023 "single queue"; section 0035-42 "virtual…several entries.; see title; a single queue)

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu and Brunheroto by using the above recited features, as taught by Kiremdjian, in order to provide a traffic-shaping cell that can control network bandwidth at very high datapacket rates and in real time, while preventing out-of order deliver (see Kiremdjian sections 0005-15). At the time of the invention the prior art discloses that a single queue is used to implement multiple virtual queues (Kiremdjian), where it would have been obvious to a person of ordinary to implement the queues of Sindhu (figure 7, 88 and / or figure 9, 104) via the sub queues of

the single queue as taught by Kiremdjian. Therefore, all the packet headers would be handled / stored by a single queue.

4. Claims 3, 17-19, 24, 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) , Brunheroto et al (US 6,643,298), and Kiremdjian et al. (US 2003/0081623) as applied to claim 1 above, and further in view of De Silva et al. (US 7,499,456)

For claim 3, 17-19, 24, 37-39, Sindhu and Brunheroto discloses the claimed invention as described above.

For claim 3, 17-19, 24, 37-39, Sindhu discloses assignment means is responsive to whereby to determine an exit order number for that packet packets (see col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory"; col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; packet header (s) are arranged and stored using request generator and queue(s) 104 in a certain exit order based on priority, which is found in the header of a packet)

.

For claim 3, 17-19, 24, 37-39 , Sindhu discloses for assigning said exit order to sorting said packets (see col 6 lines 35-50 "data cell includes a header portion…: col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory")

Sindhu, Brunheroto and Kiremdjian are silent about:

For claim 3 and similarly 24, information contained in a table

For claim 17 and similarly 37, comprising tables of information, wherein said tables are stored locally to said processor (elements)

For claim 18 and similarly 38, said tables are for the same class of service on each-said processor (elements)

For claim 19 and similarly 39, wherein said tables are for different varying classes of service on said processor (elements)

De Silva from the same or similar field of endeavor discloses the following features:

For claim 3 and similarly 24, De Silva discloses information contained in a table (see fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 17 and similarly 37, De Silva discloses comprising tables of information, wherein said tables are stored locally to said processor (elements) (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 18 and similarly 38, De Silva discloses said tables are for the same class of service on each-said processor (elements) (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 19 and similarly 39, De Silva discloses wherein said tables are for different varying classes of service on said processor (elements) (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Brunheroto and Kiremdjian by using the above recited features, as taught by De Silva, in order to provide a method which does not result in forwarding errors thus increasing efficiency of the network (see De Silva col 4.)

5. Claims 4, 21, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) , Brunheroto et al (US 6,643,298), Kiremdjian et al. (US 2003/0081623) as applied to claim 1 above, and further in view of Yazaki et al. (US 2005/0163049)

For claim 4, 21, 25, Sindhu, Brunheroto and Kiremdjian discloses the claimed invention as described above.

Sindhu, Brunheroto and Kiremdjian are silent about:

For claim 4 and similarly 25, assignment means is responsive to information associated with a data packet stream in which said packet is located whereby to determine an exit order number for that packet.

For claim 21, assignment means implements algorithms for packet scheduling in accordance with predetermined criteria, including other prioritisation and sorting.

Yazaki from the same or similar field of endeavor discloses the following features:

For claim 4 and similarly 25, Yazaki assignment means is responsive to information associated with a data packet stream in which said packet is located whereby to determine an exit order number for that packet (see claim 2 priority of the packet based on the flow identifier…buffer stores packets in order of priority"; section 0046 "each incoming packet…flow…packets").

For claim 21, assignment means implements algorithms for packet scheduling in accordance with predetermined criteria, including other prioritisation and sorting (see claim 2 priority of the packet based on the flow identifier…buffer stores packets in order of priority"; section 0046 "each incoming packet…flow…packets").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Brunheroto and Kiremdjian by using the above recited features, as taught by Yazaki, in order to provide high-speed

traffice shaping and to make efficient use of minimum bandwidth (see Yazaki sections 0004-12)

6. Claims 9-10, 30, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) , Brunheroto et al (US 6,643,298) , Kiremdjian et al. (US 2003/0081623) as applied to claim 1 above, and further in view of Donis et al. (US 2002/0075882)

For claims 9, 10, 30, 31 Sindhu, Brunheroto and Kiremdjian discloses the claimed invention as described above.

For claims 9, 10, 30, 31, Sindhu discloses the packet records packets (see col 6 lines 35-50 "data cell includes a header portion…: col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory")

For claim 9 and 10, Kiremdjian discloses a sole queue (see fig. 2a; section 0023 "single queue"; section 0035-42 "virtual…several entries.; see title; a single queue)

.

Sindhu, Brunheroto and Kiremdjian are silent about:

Regarding claim 9, and similarly 30 means to drop certain data before being output from said queue means.

Regarding claim 10, and similarly 31 dropping certain data before being queued in said queue means.

Donis from the same or similar field of endeavor discloses the following features:

Regarding claim 9, and similarly 30 Donis discloses means to drop certain data before being output from said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being queued in said queue means).

Regarding claim 10, and similarly 31 Donis discloses dropping certain data before being queued in said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being queued in said queue means).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Brunheroto and Kiremdjian by using the above recited features, as taught by Donis, in order to provide a method a priority scheme where different data types are treated differently in the network in order to satisfy the particular QoS of the data type (see Donis sections 0003-13)

7. Claims 12-16, 33-36, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) , Brunheroto et al (US 6,643,298), Kiremdjian et al. (US 2003/0081623) as applied to claim 1 above, and further in view of Wilkinson et al. (US 6,094,715)

For claim 12-16, 33-36, 46, Sindhu, Brunheroto and Kiremdjian discloses the claimed invention as described above.

Sindhu, Brunheroto and Kiremdjian are silent about:

For claim 12 and similarly 33, wherein said processor comprises a parallel processor.

For claim 13 and similarly 34, wherein said parallel processor is an array processor comprising one array of processor elements.

For claim 14 and similarly 35, wherein said array processor is a SIMD processor.

For claim 15, further comprising means to provide access for said parallel processor to shared state.

For claim 16 and similarly 36, further comprising a state engine to control said access to said shared state.

For claim 46, silicon integrated circuits.

Wilkinson from the same or similar field of endeavor discloses the following features:

For claim 12 and similarly 33, Wilkinson discloses wherein said processor comprises a parallel processor (see col 3 lines 15-55 "Array…SIMD…array processor…array processor"; col 13 line 35 "parallel array processor…SIMD…").

For claim 13 and similarly 34, Wilkinson discloses wherein said parallel processor is an array processor comprising one array of processor elements processor (see col 3 lines 15-55 "Array…SIMD…array processor…array processor"; col 13 line 35 "parallel array processor…SIMD…").

For claim 14 and similarly 35, Wilkinson discloses wherein said array processor is a SIMD processor (see col 3 lines 15-55 "Array…SIMD…array processor…array

processor"; col 13 line 35 "parallel array processor…SIMD…"; col 27 line 35-50 "state of interrupt mask…SIMD").

For claim 15, Wilkinson discloses further comprising means to provide access for said parallel processor to shared state (col. 25, lines 14-67, wherein the individual PME memory can be divided into local and shared global areas programmatically corresponds to providing access for parallel processors to shared state; col 42 line 20-35 "single CC can be shared…"; col 47 line 10-35 "elements ...share common indexing, addressing...").

For claim 16 and similarly 36, Wilkinson discloses further comprising a state engine to control said access to said shared state. (col. 25, lines 14-67, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state; col 27 line 35-50 "state of interrupt mask…SIMD").

For claim 46, silicon integrated circuits (see col 3 lines 15-55 "Array…SIMD…array processor…array processor"; col 13 line 35 "parallel array processor…SIMD…"; col 27 line 35-50 "state of interrupt mask…SIMD" Official notice I taken that processors can / are made by silicon).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Brunheroto and Kiremdjian by using the above recited features, as taught by Wilkinson, in order to provide large parallel processor and computer systems which can handle great amount of data / processes at the same time (see Wilkinson col 11)

8. Claims 48-55 rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887), Brunheroto et al (US 6,643,298), Kiremdjian et al. (US 2003/0081623) and Wilkinson et al. (US 6,094,715) as applied to claim 13/34 above, and further in view of De Silva et al. (US 7,499,456)

For claims 48-50, 52-54, Sindhu, Wilkinson and Brunheroto discloses the claimed invention as described above.

For claim 48-50, 52-54, Sindhu discloses sorting said packet records (see col 6 lines 35-50 "data cell includes a header portion…: col 9 line 10-40 "Packets received by the line card include a packet header…includes source and destination addresses…length….each header may include priority data defining a priority level associated with the corresponding packet...give preference to packets with higher priority levels"; col 10 line 10-50 "plurality of header queues…sends the packet headers to header queues…cells from a data packet having a very high priority may be loaded into the top of its associated header queue...can the transferred through the switch fabric quickly and without waiting for …when the cells arrived in system memory")

For claim 48,49,52,53, Brunheroto discloses each processor element of said parallel processor (see col 3 lines 15-55 "Array…SIMD…array processor…array processor"; col 13 line 35 "parallel array processor…SIMD…"; col 27 line 35-50 "state of interrupt mask…SIMD"); information stored locally (see col 25 line 10-67 "PME memory…local and shared ").

For claim 50, 54, Brunheroto discloses different processor elements of said parallel processor(see col 3 lines 15-55 "Array…SIMD…array processor…array processor"; col

13 line 35 "parallel array processor…SIMD…"; col 27 line 35-50 "state of interrupt mask…SIMD").

For claim 51, 55, Brunheroto discloses wherein said processor elements share information from information/state, such that:

(a) the information held in information/state in one processor element is accessible by other processing element(s) of said parallel processor (col. 25, lines 10-67, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state; col 27 line 35-50 "state of interrupt mask…SIMD").

; and (b) processor elements have access to other processor elements in said parallel processor, whereby processor elements can perform on behalf of other processor elements of said parallel processor (col. 25, lines 10-67, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state; col 27 line 35-50 "state of interrupt mask…SIMD").

Sindhu, Wilkinson and Brunheroto are silent about:

For claim 48 and similarly 52, further comprising tables of information wherein said tables are stored locally

For claim 49 and similarly 53, wherein said tables are for the same class of service

For claim 50 and similarly 54, wherein said tables are for varying classes of service

For claim 51 and 55, respective tables, perform table lookups

De Silva from the same or similar field of endeavor discloses the following features:

For claim 48 and similarly 52, De Silva discloses further comprising tables of information wherein said tables are stored locally (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 49 and similarly 52, De Silva discloses wherein said tables are for the same class of service (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 50 and similarly 52, De Silva discloses wherein said tables are for varying classes of service (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

For claim 51 and 55, De Silva discloses respective tables, perform table lookups (see fig. 3; fig. 4 ;40c, 406; fig. 8; 800a, 808; fig. 5 see col 5 lines 1-40 "on or more CoS mapping tables…identified CoS mapping table…")

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Wilkinson and Brunheroto by using the above recited features, as taught by De Silva, in order to provide a method which does not result in forwarding errors thus increasing efficiency of the network (see De Silva col 4.)

9. Claims 57, 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 7,342,887) , Brunheroto et al (US 6,643,298) , Kiremdjian et al. (US 2003/0081623) as applied to claim 56/60 above, and further in view of Williams et al. (US 7,035,908)

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Sindhu, Wilkinson and Kiremdjian do not explicitly discuss the following:

For claim 57, 61, wherein said system is implemented on a single chip.

Prabhu from the same or similar field of endeavor discloses the following features:

For claim 57, 61, Prabhu discloses wherein said system is implemented on a single chip (see col 1 lines 30-50).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify / combine the features of Sindhu, Wilkinson and Kiremdjian by using the above recited features, as taught by Williams, in order to provide method and/or architecture that provides multiple processors to enable parallel execution of software, cleaner partitioning of system software and/or increased efficiency of system bandwidth (see Williams col 1)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENAN CEHIC whose telephone number is (571)270-3120. The examiner can normally be reached on Monday through Friday 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KWANG BIN YAO can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

//Kenan Cehic/

Examiner, Art Unit 2473

/KWANG B. YAO/

Supervisory Patent Examiner, Art Unit 2473